N-Channel Enhancement Mode Power MOSFET

● Features

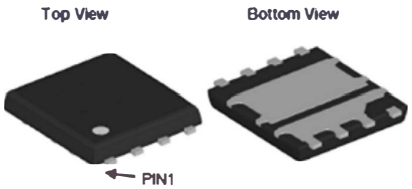
V_{DS} = 30V,

I_D = 41A

$R_{DS(ON)}$ @V_{GS}= 10V TYP 5.5mΩ

$R_{DS(ON)}$ @V = 4.5V TYP 8.5mΩ

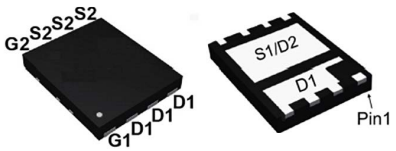
● Pin Configurations



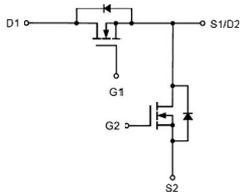
PDFN5*6-8L

● General Description

- CPU core power
- POL
- Computer / server peripherals
- Synchronous buck converter
- Telecom DC/DC



TDFN5*6-8L



N-Channel MOSFET

● Absolute Maximum Ratings @T_C=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current (Continuous) *AC	T_C=25°C T_C=70°C	I_D	41 10.4	A
Drain Current (Pulse) *B		I_{DM}	150	A
Power Dissipation	T_C=25°C	P_D	20.2	W
Operating Temperature/ Storage Temperature		T_J/T_{STG}	-55~150	℃

● Thermal Resistance Ratings

● Parameter		Maximum	Unit
Maximum Junction-to-Ambient	t ≤ 10 s	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	6.2	

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static *D						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V				μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_{DS} = 250μA			2.5	V
Gate Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$ $R_{DS(on)}$	V_{GS} = 10V, I_D = 20A V_{GS} = 4.5V, I_D = 10A		5.5 8.5	7.2 12	mΩ mΩ
Diode Forward Voltage	V_{SD}	I_{SD} = 1A V_{GS} = 0V			1.2	V
Diode Forward Current *A	I_S	T_C =25°C			16.8	A
Switching						
Total Gate Charge Gate-Source Charge Gate-Drain Charge	Q_g Q_{gs} Q_{gd}	V_{DS} = 15V I_D = 10A V_{GS} = 4.5V		14.3 2.8 1.6		nC nC nC
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 10A, V_{GS} = 10V, R_{GEN} = 1Ω		10		ns
Turn-on Rise Time	t_r			10		ns
Turn-off Delay Time	$t_{d(off)}$			15		ns
Turn-Off Fall Time				10		ns
Dynamic						
Input Capacitance	C_{iss}	V_{DS}= 15V V_{GS}=0V f=1.0MHz		1000		pF
Output Capacitance	C_{oss}			280		pF
Reverse Transfer Capacitance	C_{rss}			34		pF

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design

B: Repetitive rating, pulse width limited by junction temperature

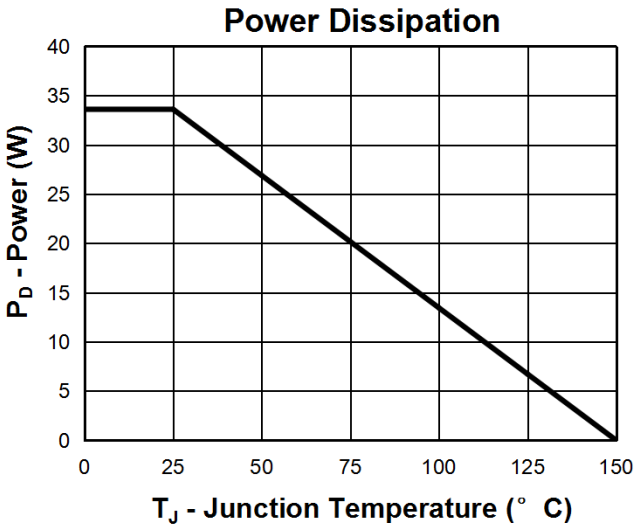
C: The current rating is based on the t≤ 10s junction to ambient thermal resistance rating.

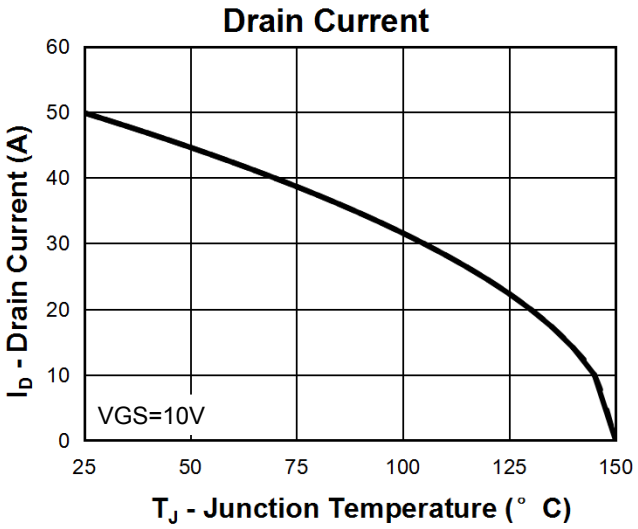
D: Pulse Test：Pulse Width≤ 300μs，Duty Cycle≤ 2%

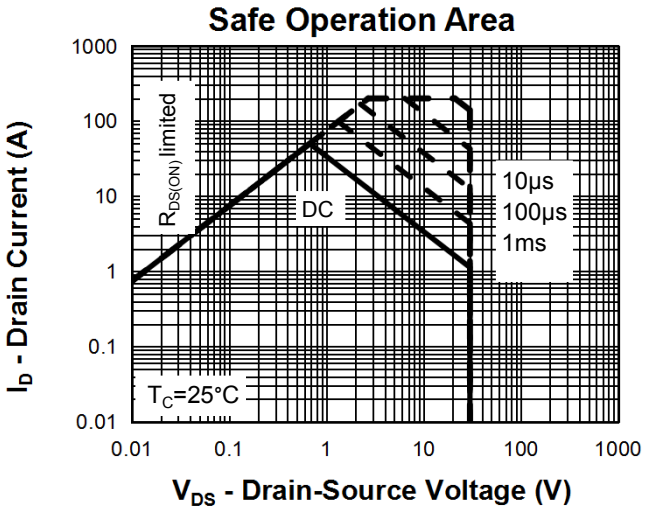
Ordering and Marking Information

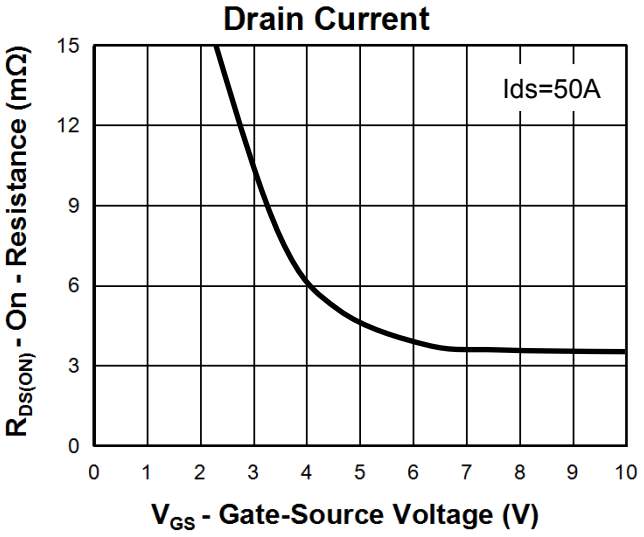
Device	Marking	Package	Packaging	Quantity	Reel Size	Tape width
XPX7492RD	XPX7492RD	PDFN5060	Tape&Reel	5000	13"	12mm

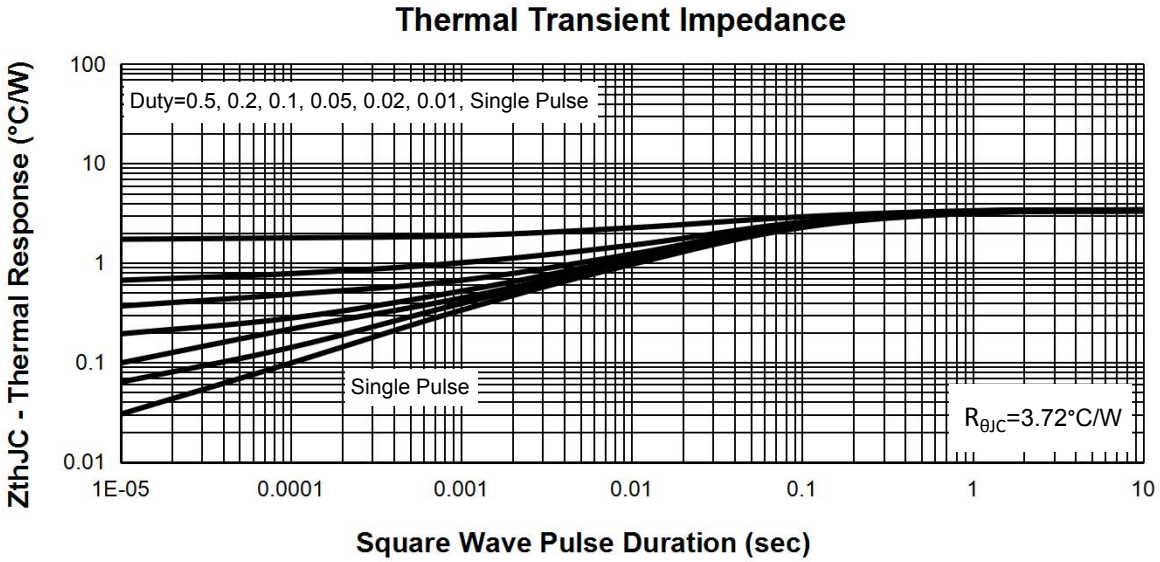
Typical Characteristics





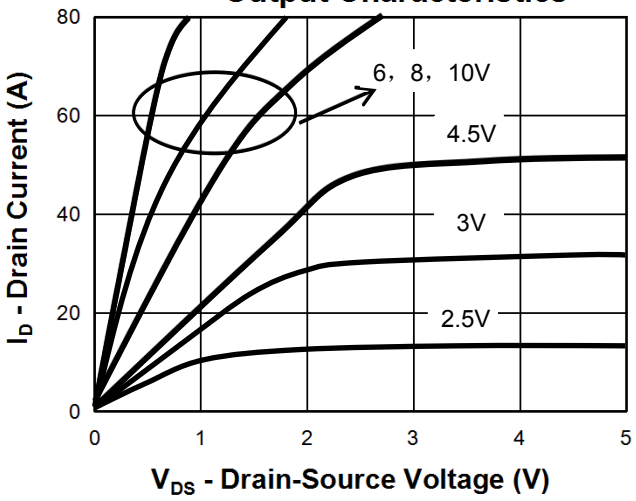




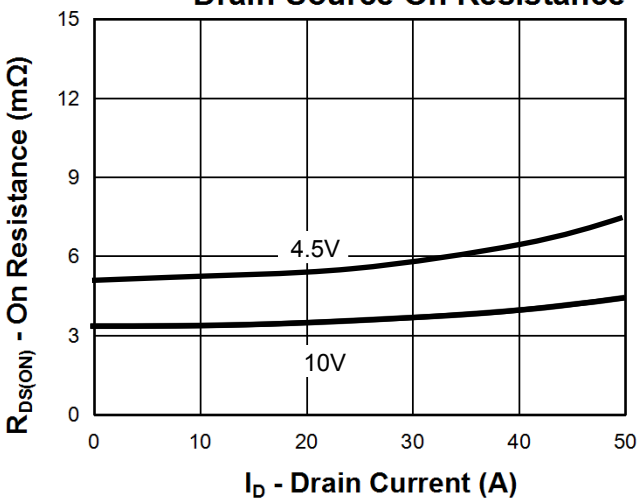


Typical Characteristics

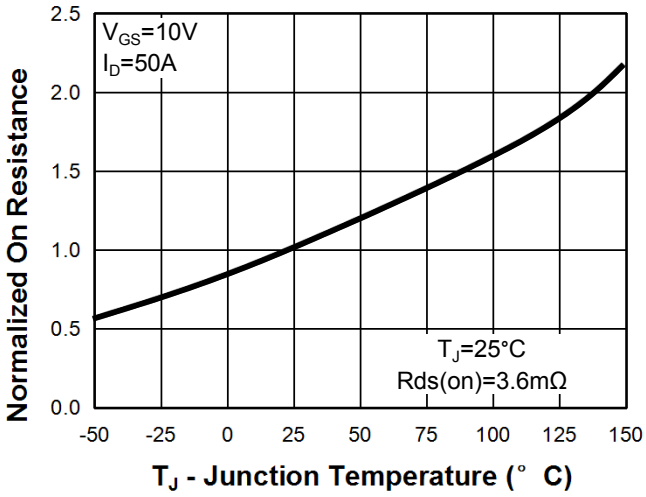
Output Characteristics



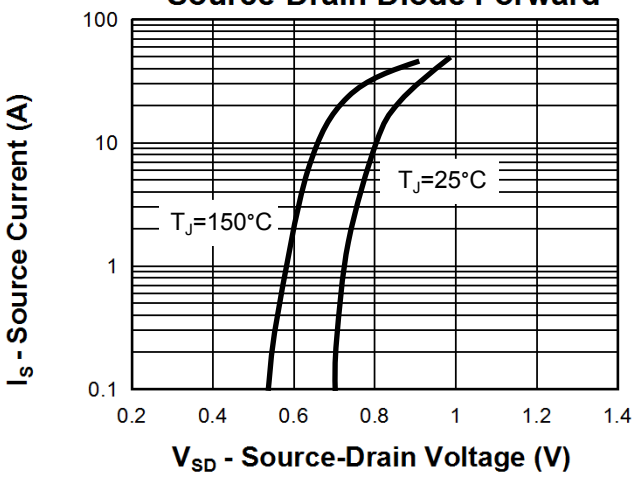
Drain-Source On Resistance



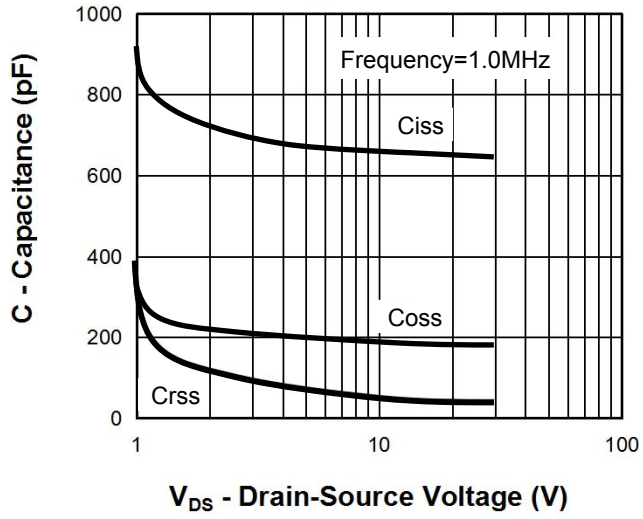
Drain-Source On Resistance



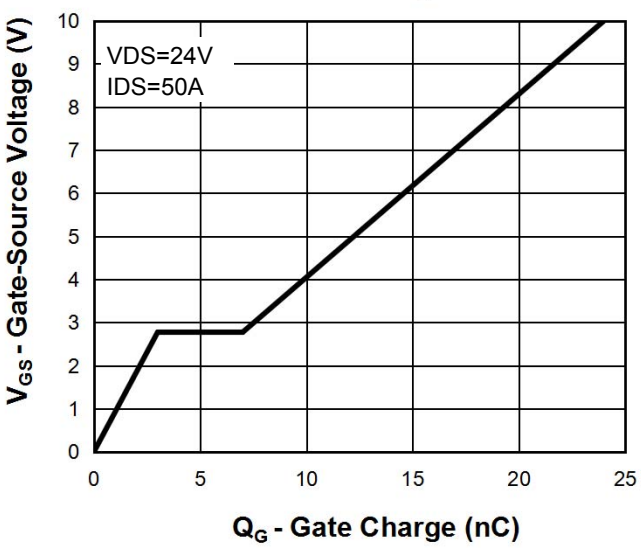
Source-Drain Diode Forward



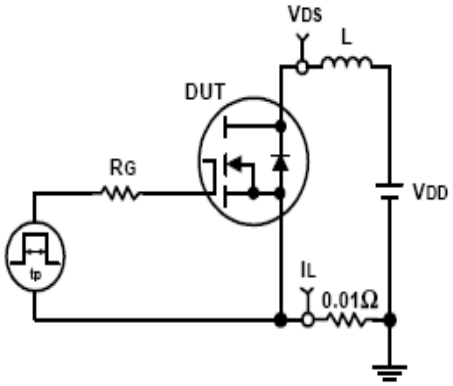
Capacitance

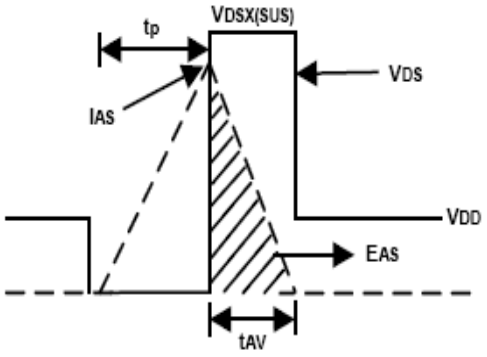


Gate Charge

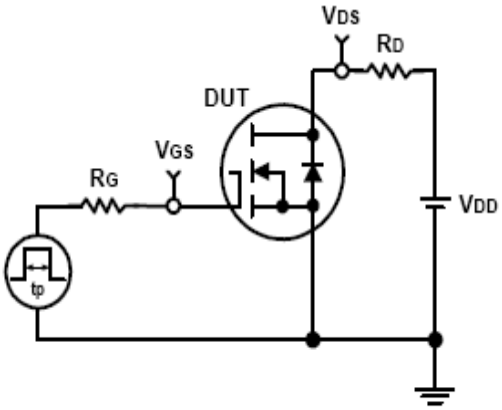


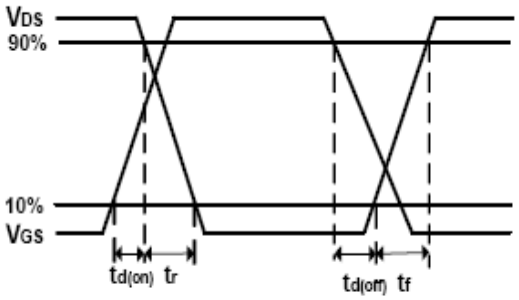
Avalanche Test Circuit and Waveforms





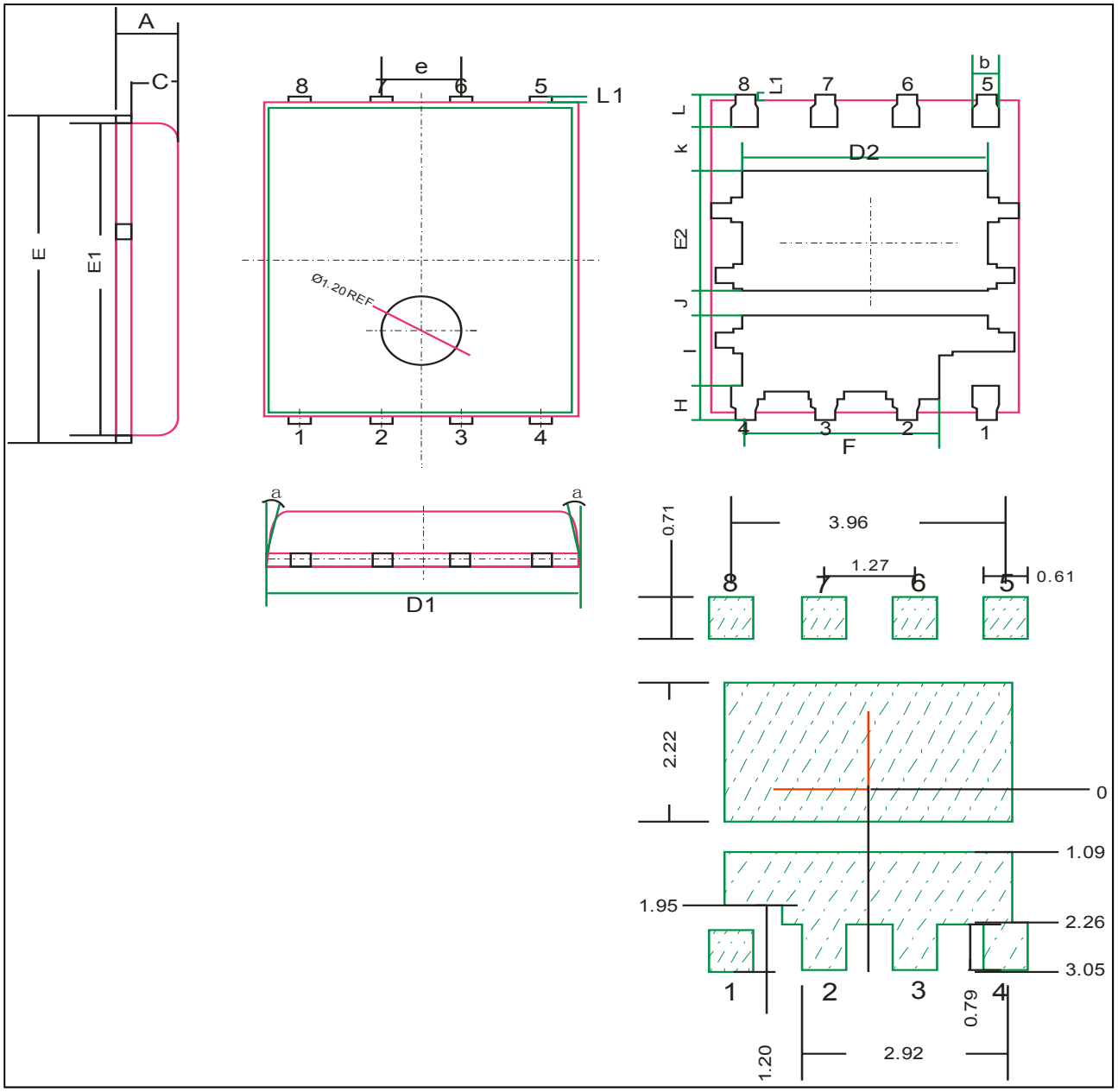
Switching Time Test Circuit and Waveforms





Package Information

PDFN5060



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043	E1	5.70	5.75	5.80	0.224	0.226	0.228
b	0.33	0.41	0.51	0.013	0.016	0.020	E2	2.02	2.17	2.32	0.079	0.085	0.091
c	0.20	0.25	0.30	0.008	0.010	0.012	e	1.27BSC			0.05BSC		
D1	4.80	4.90	5.00	0.189	0.193	0.197	H	0.48	0.58	0.68	0.018	0.022	0.026
D2	3.61	3.81	3.96	0.142	0.150	0.156	L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008							
E	5.90	6.00	6.10	0.232	0.236	0.240	@	0°	*	12°	*	10°	12°
K	0.50	*	*	0.019	*	*	J	0.40	0.50	0.60	0.015	0.019	0.023
I	1.22	1.32	1.42	0.048	0.051	0.055	F	2.87	3.07	3.22	0.112	0.12	0.126

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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